D 72981 (Pages : 2) Name.....

Reg. No.....

# FIRST SEMESTER M.A./M.Sc./M.Com. DEGREE EXAMINATION DECEMBER 2019

(CBCSS)

Physics

PHY 1C 04—ELECTRONICS

(2019 Admissions)

Time : Three Hours Maximum : 30 Weightage

## Section A

*Answer* **all** *questions.*
*Each question carries weightage* 1.

1. What is Multi-vibrator ? Classify them.
2. Write all the four different types of filters ?
3. Briefly explain zener and avalanche breakdowns.
4. Explain 3 dB cutoff frequency ? Why is it 3 dB, not 1 dB ?
5. What is Positive logic and Negative Logic ?
6. Obtain the expression for loop gain of an inverting amplifier using Op-amp.
7. Write a short note on LDR.
8. How can you convert a JK Flip-flop to a Register ?

(8 × 1 = 8 weightage)

## Section B

*Answer any* **two** *questions.*
*Each question carries weightage* 5.

9. With the help of a logic diagram explain the working of a 4 bit right shift register.
10. Explain the working of a second order low pass and high pass Butterworth filter with the help of circuit diagram.
11. Explain the different biasing techniques used in JFET and also explain the working of a common drain amplifier.
12. Give the structure and operation of depletion MOSFET. How is depletion MOSFET different from enhancement MOSFET ? With the help of a circuit explain the working of a NOT Gate.

(2 × 5 = 10 weightage)

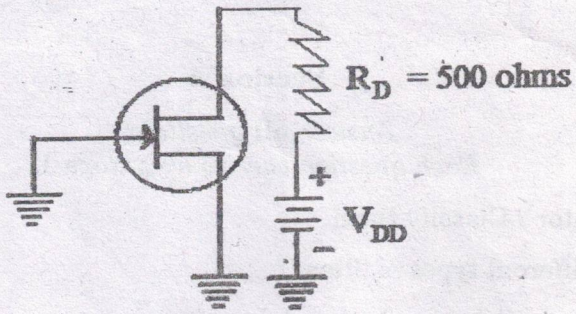
Turn over

## Section C

*Answer any* **four** *questions.*
*Each question carries weightage* 3.

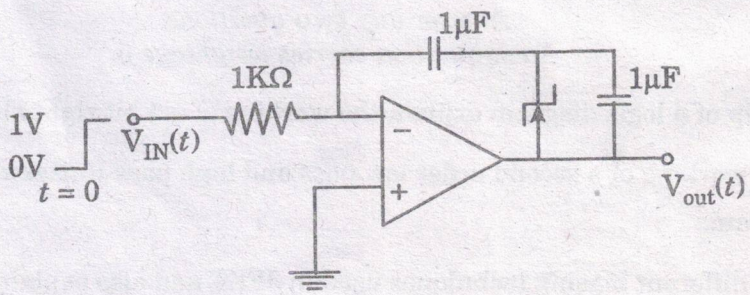
13. Show how an asynchronous counter can be implemented having a modulus of 9 with a straight binary sequence from 0000 through 1000.

14. For the JFET in the given figure, $V_{GS(off)}$ is – 6V and $I_{DSS}$ is 15 mA. Determine the minimum value of $V_{DD}$ required to put the device in constant current area of operation.




15. Design a practical differentiator that will differentiate signals with frequencies up to 400 Hz. The gain at 10 Hz should be 0.12. If the op-amp used in the design has a unity gain frequency of 2 MHz, what is the upper cutoff frequency of the differentiator ?

16. In the circuit shown below, the op-amp is ideal and Zener voltage of the diode is 2.5 volts. At the input, unit step voltage is applied, i.e. $V_{IN}(t) = u(t)$ volts. Also, at $t = 0$, the voltage across each of the capacitors is zero. Find the time '$t$' in milliseconds, at which the output voltage $V_{OUT}$ crosses the Zener break down.




17. Using Karnaugh Map solve the given equation to reduce the number of gates used.

$$Y = ABCD + \bar{A}BCD + AB\bar{C}D + AB\bar{C}\bar{D}.$$

18. In the figure given below assume the ideal op amp is used. Find the output voltage if an input signal Vs = 15 cos (50t) is applied.

19. Draw the logical circuit of an synchronous decade counter.

(4 × 3 = 12 weightage)